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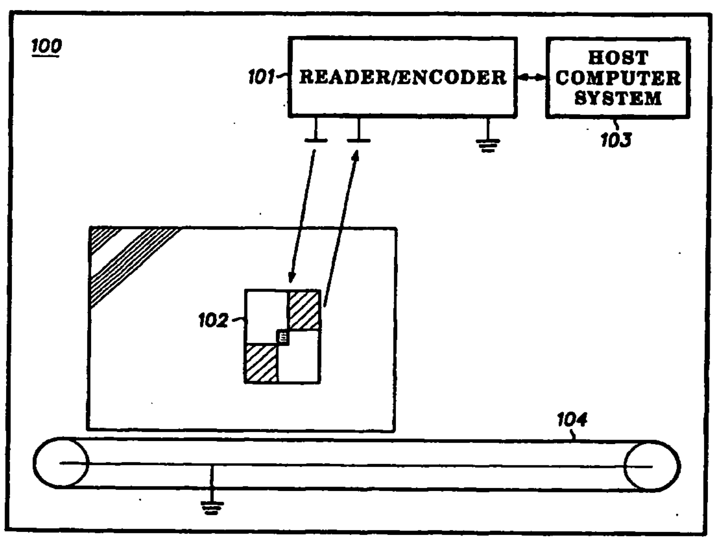

(57) Abstract

A contactless programmable electrostatic RFID apparatus (101, 102) that is cost–effective, has high manufacturability, and can be easily packaged for a wide range of applications is presented. Under the present invention, following an exciter signal, a data reader/encoder (101) transmits a write mode data sequence to communicate to a transponder (102) whether to enter into write mode. The modulated write mode data sequence further provides instruction, data, and memory address information for the transponder to use in writing data into its memory. Conversely, the transponder interprets the absence of such write mode data sequence to mean that read mode is desired. Accordingly, read mode is the default mode.

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ELECTROSTATIC RADIO FREQUENCY IDENTIFICATION SYSTEM HAVING CONTACTLESS PROGRAMMABILITY

Field of the Invention

The invention generally relates to Radio Frequency Identification (RFID) technology, and more particularly relates to contactless programmable electrostatic RFID technology.

Cross Reference to Related Applications

This is a continuation-in-part of United States patent application Serial No. 09/061,146, filed 16 April 1998, Attorney Docket No. IND00701P01, assigned to Motorola, Inc.

Background of the Invention

Radio Frequency Identification (RFID) technology allows identification data to be transferred remotely which provides a significant advantage in identifying persons, articles, parcels, and others. In general, to access identification data stored in an RFID transponder (e.g., an RFID "tag") remotely, a RFID reader/encoder generates an energy field to activate the RFID transponder and subsequently to retrieve data stored in the transponder unit from a distance. The data retrieved is then processed by a host computer system to identify the person or article that is associated with the transponder. A transponder that derives its power from the energy field is known as a passive transponder, while a transponder that has its own power source is known as an active transponder. RFID technology has found a wide range of applications including tracking, access control, theft prevention, security, etc.

For some applications, RFID technology is more preferable than magnetic strip technology, which also finds applications in a few of the areas above. Generally, RFID technology allows for storing more information than magnetic strip technology, because magnetic strip technology as commonly deployed has very limited memory capability. Moreover, magnetic strip technology requires relatively high maintenance (e.g., head cleaning). Furthermore, magnetic strip technology is prone to moisture damage, dust damage, magnetic field damage, etc.

RFID technology should be distinguished from Radio ID technology which uses ordinary radio waves, or more precisely far field electromagnetic (EM) waves. Far field means the distance between the transceiver and transponder is great

compared to the wavelength of the EM carrier signal used. An example of Radio ID technology is the Identify Friend or Foe (IFF) systems used with military aircraft. Far field EM waves have a field strength that varies inversely with the distance involved.

In contrast, conventional RFID technology is based upon inductive coupling utilizing magnetic field waves. Conventional RFID technology operates in the near field where the operating distance can be far less than one wavelength of the EM field. Unlike far field radio waves, the magnetic field strength in the near field is approximately proportional to the inverse cube of the distance from the source. In inductance-based RFID technology, the electromagnetic field can be used both as a power source for the transponder and for transferring data and clock information between the reader/encoder and transponder. Magnetic fields are generated by causing RF alternating current to flow in coils that typically have multiple turns. However, it is difficult to integrate these coils in an integrated circuit. Generally, these coils are required to be wire windings or etched metal. This requirement adversely impacts the costs, manufacturability, and packaging flexibility of inductance-based RFID technology. Due to the prohibitive costs and high degree of manufacturing difficulty, electromagnetic RFID technology is not practical in high volume/low cost disposable applications. The bulky packaging, which is typical for electromagnetic RFID technology, further limits its application to those where thickness is not of primary importance.

Conventional electromagnetic RFID technology provides the capability to contactlessly program a transponder with the desired information. Such programmability is desirable because it allows manufacturers to implement unprogrammed RFID tags into application specific product packaging, which can be programmed at a later and more opportune time by others in the chain such as distributors, retailers, or end users. Contactless programmability is also desirable because it allows for programming to be performed anywhere with a minimum amount of equipment and set-up.

Thus, a need exists for an RFID system that allows for contactless programming, that is cost-effective, has high manufacturability, can be easily packaged for a wide range of applications, and that is operationally robust.

Summary of the Invention

Accordingly, the present invention provides a contactless programmable RFID apparatus, system, and method that is cost-effective, has high manufacturability, can be easily packaged for a wide range of applications, and operationally robust.

The present invention meets the above need with an electrostatic Radio Frequency Identification (RFID) system that is capable of bi-directional data transfer between an electrostatic RFID reader/encoder circuit and a plurality of electrostatic RFID transponder circuits.

The RFID reader/encoder circuit comprises a processor, an exciter circuit coupled to the processor, and a first plurality of electrodes coupled to the exciter circuit. The exciter circuit electrostatically generates and transmits an RF exciter signal over the first plurality of electrodes. In addition, the exciter circuit further generates and transmits an RF signal carrying a data sequence received from the processor. The data sequence carries information to indicate whether write mode is involved as well as instruction, data, and address information related to a desired operation (e.g., write or read operation). The data sequence may also include a lock bit. In accordance to the present invention, the data sequence is a transmitted modulation and is composed of a sequence of blanking gaps and pulses. The pulses represent binary values and their duration determines whether it is a zero (0) or a one (1). Under the present invention, the data sequence indicates a write operation if the data sequence begins with a blanking gap.

Each of the plurality of RFID transponder circuits comprises a plurality of electrostatic electrodes; an analog interface module coupled to the electrostatic electrodes; memory; a controller coupled to the analog interface module and the memory, a modulator coupled to the controller, the memory, and the analog interface module; and a write decoder coupled to the controller and the analog interface module. The analog interface module is used to extract the exciter signal, the clock signal, and the data sequence signal from a RF signal received by the plurality of electrostatic electrodes. The analog interface module rectifies and regulates the exciter signal for use in activating the transponder circuit. The analog interface module detects whether a read or a write command is involved. The controller writes data information from the data sequence signal into memory in response to a write command. The controller reads data information from memory and sends the read data information to the modulator for modulation in response to a read command. The modulated data is then sent to the analog interface module for transmitting over the plurality of electrostatic electrodes.

All the features and advantages of the present invention will become apparent from the following detailed description of its preferred embodiment whose description should be taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a high-level block diagram illustrating an exemplary electrostatic Radio Frequency Identification (RFID) system that implements the present invention.

FIG. 2 is a block diagram illustrating in greater detail the electrostatic RFID reader/encoder 101 illustrated in FIG. 1.

FIG. 3 is a block diagram illustrating in greater detail the electrostatic RFID transponder (tag) 102 illustrated in FIG. 1.

FIG. 4 is a block diagram illustrating in greater detail the analog interface module 301 illustrated in FIG. 3.

FIG. 5 illustrates a schematic diagram of a load modulation circuit 309 which is used in the reflective load modulation scheme in accordance with the present invention.

FIG. 6 illustrates an exemplary mapping of the contents of memory 310.

FIG. 7 illustrates the lock bit and the individual configuration bits from the configuration block (block 0) of memory 310.

FIG. 8 is a flow chart illustrating the principal steps involved in bi-directional data transfer between reader/encoder 101 and transponder 102 in accordance with the present invention.

FIG. 9 illustrates, as an example, the differential voltage between pads 312 and 313 in write mode in accordance with the present invention.

FIG. 10 illustrates, as an example, the differential voltage between pads 312 and 313 in read mode in accordance with the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention. While the following detailed description of the present invention describes its application to

passive transponders (i.e., without their own power source), it is to be appreciated that the present invention is also applicable to active transponders (i.e., with their own power source). Furthermore, while the following detailed description of the present invention is related to monopole systems, it is to be appreciated that the present invention is also applicable to dipole systems.

The Radio Frequency Identification (RFID) technology implemented under the present invention is capacitance-based. In capacitance-based RFID technology, an electrostatic field is generated for use in activating the electrostatic RFID transponder (e.g., "tag") and transmitting information between the electrostatic RFID reader/encoder and electrostatic RFID transponder. In short, an electrostatic field is an energy (electrical) field created between two electrodes having a voltage differential. Because electrodes (i.e., plates) are used (instead of coils) to transmit and receive electrostatic signals, capacitance-based RFID technology can be implemented in an integrated circuit. The electrodes and associated electrical circuits of electrostatic RFID systems can easily be implemented on flat and printable surfaces including paper, plastic, or synthetic substrates. Moreover, the manufacturing process involved is inexpensive and requires minimal components and set-up. As such, electrostatic RFID technology may be ideal for disposable applications. Furthermore, contactless electrostatic programmability is provided in accordance to the present invention.

FIG. 1 illustrates, for example, a system level diagram of an electrostatic RFID system in accordance to the present invention. In accordance to the present invention, electrostatic RFID system 100 allows for contactless bi-directional signal transfer between a reader/encoder and transponder. More particularly, electrostatic RFID system 100 is a parcel/letter tracking system in which packages or letters placed on a conveyor belt are automatically tracked to determine identification information including sender's name and address, receiver's name and address, date ship, check-in station, time stamp, etc. It is to be appreciated that electrostatic RFID system 100 is exemplary only and that the present invention can be implemented in a number of different electrostatic RFID systems including an inventory management system, an identification access system, an admission ticketing system, etc.

As shown in FIG. 1, electrostatic RFID system 100 includes electrostatic RFID reader/encoder 101, electrostatic RFID transponder 102, host computer system 103, and conveyor 104. Electrostatic RFID transponder 102 may comprise one of a plurality of electrostatic RFID transponders that have been implemented as part of the

shipping labels which have been attached to the letters and packages. In accordance to the present invention, each electrostatic RFID transponder 102 can be programmed to store the desired information on site where the label to which it is attached is generated. In other words, electrostatic RFID reader/encoder 101 can provide bi-directional data transfer to/from electrostatic RFID transponder 102 and vice versa. In the preferred embodiment, such programming can be performed using electrostatic RFID reader/encoder 101 or a programming unit that is substantially similar in function. Conveyor 104 is set up so that the letters and packages when placed on the conveyor are within transmission range of electrostatic RFID reader/encoder 101 and electrostatic RFID transponder 102. The letters and packages placed on conveyor 104 are moving at a speed that allows sufficient time for the information to be read.

In general, electrostatic RFID reader/encoder 101 generates an electrostatic (electric) field for use both as a power/clock source for electrostatic RFID transponder 102 and for transferring information between electrostatic RFID reader/encoder 101 and electrostatic RFID transponder 102. As such, electrostatic RFID reader/encoder 101 electrostatically generates and transmits a RF power signal to the surrounding area through the reader/encoder electrodes. The RF power signal activates electrostatic RFID transponder 102 when the package to which it is attached comes within the transmitting range of reader/encoder 101. Upon being sufficiently energized, electrostatic RFID transponder 102 responds by electrostatically transmitting a RF read data signal carrying the information stored in its memory to electrostatic RFID reader/encoder 101 (as part of a read operation). In accordance with the present invention, electrostatic RFID reader/encoder 101 also electrostatically transmits a RF write signal to communicate and write information to electrostatic RFID transponder 102 (as part of a write operation). Alternatively, such programming can be carried out by a separate programming unit. It is to be appreciated that the RF power signal transmitted by electrostatic RFID reader/encoder 101 powers electrostatic RFID transponder 102 during its read and/or write operations.

The RF read signal received by electrostatic RFID reader/encoder 101 is filtered, amplified, and demodulated. The data carried by the RF read signal is retrieved and formatted as required prior to being transferred to host computer system 103. Upon receiving the formatted data, host computer system 103 may use the data to update its database. In the current example, host computer system 103 may update the information in its database to reflect the latest status of a package. Host computer

system 103 may further processes the information received as required in a different application. For example, in an access ID application, host computer system 103 may compare the information received with those already stored in its database to determine whether access should be granted or denied to the individual.

FIG. 2 illustrates in greater detail the components of electrostatic RFID reader/encoder 101. As shown in FIG. 2, electrostatic RFID reader/encoder 101 comprises exciter 201, receiver 202, demodulator 203, processor 204, exciter electrode 205, and receiver electrode 206. Exciter electrode 205 is coupled to exciter 201. In a dipole configuration, there is a first exciter electrode and a second exciter electrode. In a monopole configuration which is shown in FIG. 2, the second exciter electrode is connected to ground. Likewise, receiver electrode 206 is coupled to receiver 202. In a dipole configuration, there is a first receiver electrode and a second receiver electrode. In a monopole configuration which is shown in FIG. 2, the second receiver electrode is connected to ground. In a read operation, exciter 201 generates a RF exciter signal (via exciter electrode 205) for activating electrostatic RFID transponder 102. Basically, the RF exciter signal provides operating power to transponder 102 in the form of electrostatic energy. In addition, the carrier frequency of the RF exciter signal provides clock information for transponder 102. In the preferred embodiment, the RF exciter signal has a carrier frequency of 125 kHz. The exciter signal is transmitted to electrostatic RFID transponder 102 through exciter electrode 205. Additionally, exciter 201 may further generate and transmit a RF signal which carries a read mode data sequence including instruction, data, and address information related to a read operation to immediately follow the exciter signal. In response, transponder 102 sends back the data stored in its memory.

Upon receiving an electrostatic RF read data signal from electrostatic transponder 102 via receiver electrode 206, receiver 202 first filters out unwanted frequency bands. Receiver 202 also amplifies the RF read data signal. Receiver 202 then provides the electrostatic RF read data signal to demodulator 203 which demodulates the read data signal according to a predetermined demodulation scheme to retrieve the RF read data. In the preferred embodiment, the RF read data signal is modulated by a Phase Shift Keying (PSK) modulation scheme. It is to be appreciated that other modulation schemes such as Amplitude Shift Keying (ASK) modulation, Frequency Shift Keying (FSK) modulation, and others can also be used to modulate the RF read data signal. The electrostatic RF read data signal is then sent to processor

204 which formats the data as required by host computer 103. The formatted read data is then sent to host computer 103 for processing.

Conversely, in a write operation, formatted write data from host computer 103 is provided to processor 204 which strips all formatting information from the write data. The 'bare' write data is then provided to exciter 201 which further amplifies it prior to transmitting it to transponder 102 via exciter electrode 205. In such transmission, command and control instructions (e.g., operation codes, lock bit, etc.), data, and memory address information are encoded into a write mode data sequence which generally allows transponder 102 to distinguish whether a write operation or a read operation is desired by reader/encoder 101. As a result, the write mode data sequence includes configuration, instruction, data, and address information related to a write operation. In short, exciter 201 generates and transmits a RF signal carrying a write mode data sequence at a predetermined time following the generation and transmission of the RF exciter signal. As will be discussed later, this predetermined time is the time needed to load configuration (mode) data from memory 310 into mode register 308.

As discussed earlier, a read mode data sequence, which is distinguishable from the write mode data sequence, can also be similarly created. In the preferred embodiment, a write mode data sequence is composed of a sequence of alternating blanking gaps and pulses. The write mode data sequence begins with a blanking gap (start gap). Accordingly, a data sequence indicates a write operation if it begins with a blanking gap. The pulses represent binary values and the duration of a pulse determines whether it is a binary zero (0) or one (1). Conversely, a read mode data sequence is a sequence of dampened and non-dampened pulses.

Reference is now made to FIG. 3 illustrating in greater detail the components of transponder 102. As shown in FIG. 3, transponder 102 comprises analog interface module 301, Power On Reset (POR) circuit 302, bitrate generator 303, write decoder 304, optional charge pump 305, input register 306, controller 307, mode register 308, modulator 309, memory 310, pads/terminals 312-313, and electrostatic transponder electrodes 314 and 316. Electrostatic transponder electrodes 314 and 316 are connected to pads 312 and 313, respectively. Accordingly, pads 312-313 are used to couple transponder 102 to a RF excitation source via transponder electrodes 314 and 316. Moreover, since the RF exciter signal from reader/encoder 101 has a carrier signal that can be used as a clock signal, transponder electrodes 314 and 316 provide the coupling to allow clock information to be sent to transponder 102 for

synchronization purposes instead of requiring a clock oscillator. As such, pads 312-313 are sometimes known as clock pads. Furthermore, pads 312-313 provide the connection to transponder electrodes 314 and 316 to allow read data to be transmitted from transponder 102 to reader/encoder 101. For optimum electrostatic performance, the input capacitance between pads 312-313 is minimized. In the preferred embodiment, the input capacitance is kept at or below 5 pF. Internal bypass capacitance is provided for power reserve and for filtering out voltage ripple. Pads 312-313 are preferably located at each far end of the silicon.

Analog interface module 301 is coupled to pads 312-313 and used to extract the RF exciter signal, clock signal, and data sequence signal from a RF signal received by plurality of electrostatic transponder electrodes. As discussed earlier, the data sequence such as a write mode data sequence carries functional information. FIG. 4 is a block diagram of analog interface module 301. As shown in FIG. 4, analog interface module 301 consists of full-wave rectifier circuit 401, regulator circuit 402, clock extraction circuit 403, gap detector circuit 405, and ESD protection circuit 406. ESD protection circuit 406 is designed to provide Electrostatic Discharge (ESD) protection for transponder 102. Accordingly, any signals on pads 312-313 are governed by ESD protection circuit 406. RF signals received from pads 312-313 are passed from ESD protection circuit 406 to full-wave rectifier circuit 401 which converts the input alternating-current (ac) voltage signal supplied by pads 312-313 into a direct-current (dc) voltage. The dc voltage is provided to regulator circuit 402 which ensures that the voltage level of the dc voltage stays within a desired range. The regulated voltages Vdd and Vss are used to power electrostatic transponder 102. Clock extraction circuit 403 extracts a clock signal from the RF exciter signal. This extracted clock signal is provided throughout transponder 102. In the preferred embodiment, clock extraction circuit 403 has a clock divider circuit to generate a second clock signal that has a carrier frequency that is half of the exciter carrier frequency (i.e., 62.5 kHz). This second clock signal is eventually provided to modulator 309 (via controller 307) to use as a carrier signal in sending data from transponder 102 to reader/encoder 101.

Gap detector circuit 405 is used to detect whether there is a start or field gap in the write data sequence received from reader/encoder 101 to transponder 102 during a write mode. Such gaps indicate that a write mode is likely involved. If a start gap is detected, gap detector circuit 405 passes the write data sequence to write decoder 304. Otherwise, gap detector circuit 405 notifies controller 307 that a read mode is

involved. In essence, gap detector circuit 405 of analog interface module 301 determines whether a write or a read operation is involved. Modulator circuit 309 is used to provide load modulation dampening for sending read data signals from transponder 102 to reader/encoder 101 during read mode. FIG. 5 illustrates the relevant components residing in modulator 309 that are used to perform load modulation dampening. As shown in FIG. 5, the load modulation circuit comprises inverter 501, resistor 502, and N-type MOSFET transistor 503. Inverter 501 receives as inputs the second clock signal and data from memory 310 to drive the modulation circuit. The gate of N-type MOSFET transistor 503 is connected to the output of inverter 501, the source of N-type MOSFET transistor 503 is connected to transponder electrode 316, and the drain is connected to resistor 502 which in turned ins connected to transponder electrode 314. As such, transistor 503 is used to dampen the differential voltage across transponder electrodes 314 and 316. In other words, the impedance across the two electrodes is varied thereby introducing a voltage dampening in the differential voltage as desired.

Referring now back to FIG. 3, controller 307 controls access to memory 310. More particularly, under the right conditions, controller 307 writes data information from the write mode data sequence signal into memory 310 in response to a write command or retrieves (reads) data information from memory 310 and sends it to modulator 309 for modulation in response to a read command. Modulator 309 modulates read data retrieved from memory 310 by controller 307 according to a predefined modulation scheme. In the preferred embodiment, the modulation scheme is PSK. Modulator 309 then sends the modulated data signal to analog interface module 301 to relay to pads 312-313 which ultimately transmit the modulated read data signal to reader/encoder 101 via transponder electrodes 314 and 316.

POR circuit 302 monitors the RF exciter signal which has been rectified and regulated to determine whether a sufficient voltage has been generated to power on electrostatic RFID transponder 102. When such voltage has been built up, POR 302 allows transponder activities to begin. In other words, following reception of a RF exciter signal, POR circuit 302 determines whether a predetermined voltage threshold has been reached by the dc voltage signal generated by analog interface module 301 to power on the electrostatic RFID transponder. When this threshold is reached, POR circuit 302 asserts the enable signal to so indicate. Otherwise, the enable signal is deasserted. This enable signal is provided to all major functional circuits of transponder 102 such as controller 307 to enable or disable the circuits. Bitrate

generator 303 receives as input the clock signal having a carrier frequency of 125 kHz from clock extraction circuit 403. Bitrate generator 303 generates the data transfer rate at which data is transferred from/to memory 310 during read and write mode, respectively. In the preferred embodiment, bitrate generator 303 generates the data transfer rate by dividing the carrier frequency of 125 kHz by a predetermined factor. Alternatively, bitrate generator 303 generates the data transfer rate by multiplying the carrier frequency by predetermined factor. The data transfer rate is provided to controller 307. In the preferred embodiment, bitrate generator 303 can be configured to operate at either 125 kHz/16 (7.81 kHz) or 125 kHz/32 (3.91 kHz).

As discussed earlier, when gap detector 405 detects a blanking gap at the start of the data sequence signal following the RF exciter signal, it forwards the data sequence signal to write decoder 304. In other words, write decoder 304 only receives the data sequence signal if a write operation is involved. Write decoder 304 then decodes the data sequence signal to retrieve instruction, data, and address information related to the write operation. If it recognizes the codes as a write command, write decoder 304 signals to so notify controller 307. Write decoder 304 also verifies the validity of the data stream. The decoded instructions and information about the validity of the data stream are provided to controller 307.

In the preferred embodiment, memory 310 is an Erasable Programmable Read Only Memory (EEPROM) which has a capacity of 1,056 bits. Memory 310 is used to store write data received from reader/encoder 101 during write mode. The data is retrieved from memory 310 and sent to reader/encoder 101 during read mode. In general, relatively high voltage is required to write data into an EEPROM. Because such voltage generally takes time to build up, the write data is first buffered in input register 306. In so doing, controller 307 is free to perform other tasks in the interim period. When the required write voltage is reached, the write data buffered in input register 306 is written into memory 310. In general, controller 307 controls all read and write memory access transactions. In addition, controller 307 loads configuration information from the designated configuration (mode) memory block (block 0 of memory 310) into mode register 308. Such configuration block data is programmed in block 0 of memory 310 during the write mode and includes the operation (OP) codes as well as other configuration information that controller 307 and modulator 309 are required to follow during a read operation. Accordingly, controller 307 and modulator 309 access the op-codes and configuration information stored in mode register 308 whenever necessary.

During read mode, modulator 309 carries out the selected modulation scheme on read data retrieved from memory 310. The modulated read data signal is then sent to analog interface module 301. In the preferred embodiment, load modulation is PSK modulation. The modulation scheme can also be disabled.

Reference is now made to FIG. 6 illustrating an exemplary mapping of memory 310, which as discussed earlier, has a capacity of 1,056 bits. As illustrated in FIG. 6, memory 310 is organized into N individually addressable memory blocks each having a lock bit and 32 data bits. The first memory block (block 0) is designated as the configuration/mode block for storing configuration (mode) information which includes a lock bit and configuration bits. The remaining memory blocks are designated for storing user data which includes a lock bit, synchronization bits, and user data bits. FIG. 7 illustrates the lock bit and some exemplary individual configuration bits in the configuration block (block 0). As shown in FIG. 7, the configuration (mode) information includes a locking information bit, POR delay information, data rate information, modulation type information, modulation enable information, max block information, and modulation threshold information, etc. The lock bit of the configuration block and user blocks indicates whether the contents of the associated block can be altered. When the lock bit asserted, the lock bit and the remaining content of the associated block can not be altered. Otherwise, the lock bit and the remaining content of the associated block can be rewritten (programmed). The data rate information indicates whether bitrate generator 303 is to operate at a data rate of either 7.81 kHz or 3.91 kHz. The modulation information indicates the type of modulation. The modulation enable information enables/disables modulation. The modulation threshold information indicates the degree of modulation to be carried out. The data rate information indicates the desired data rate.

The max block information ('MAXBLK'), indicates the number of user data blocks (i.e., from block 1-to-block MAXBLK) to be cyclically transmitted to reader/encoder 101 in a read operation. MAXBLK can be any value between 0 and N. In read mode, data from memory 310 is serially transmitted beginning with bit 1 of block 1 and ending with bit 32 of block MAXBLK. The data transmission of block 1 to block MAXBLK then repeats continuously in a cyclical fashion. For example, if MAXBLK is set to six (6), blocks 1-6 are cyclically and continuously transmitted. The contents of configuration block 0 is normally not transmitted. However, if MAXBLK is set to zero (0), the contents of configuration block 0 can be read. Under the present invention, the information in configuration block 0 as well as all user data

blocks 1-N are programmable by reader/encoder 101 or a substantially similar programming unit.

Operationally, reader/encoder 101 decides whether transponder 102 is in write mode or read mode. Reader/encoder 101 transmits predetermined write mode data or read mode data sequences so indicating to transponder 102. Referring now to FIG. 8 illustrating a flow chart summarizing the principal steps involved in bi-directional data transfer between reader/encoder 101 and transponder 102 in accordance to the present invention. Regardless of whether it is a read or write operation, the first step requires reader/encoder 101 to generate and send an exciter signal to power transponder 102. Accordingly, transponder 102 monitors pads 312-313 to determine whether an exciter signal has been received (step 801). If no exciter signal has been received, transponder 102 keeps monitoring. Otherwise at power-on, transponder 102 loads configuration (mode) information from block 0 of memory 310 into mode register 308 (step 802). Gap detector 405 determines whether a start gap has been detected in the incoming data sequence (step 803). If a start gap is detected indicating that the write mode is likely involved, information from the write mode data sequence are further examined (step 804) by write decoder 304 to make certain that a write command is actually involved (step 805).

In the preferred embodiment, a communication protocol is adopted by reader/encoder 101 and transponder 102 to communicate whether a write command is actually involved. Such communication protocol is embodied in the so-called write mode data sequence. In addition to indicating that a write command is actually involved, the write mode sequence also provides the programming instruction, the programming data, and the block address. Under this protocol, the duration of the gaps (e.g., start gap and field gap) is between 50-to-400 ms. The start gap may be longer than the subsequent field gaps to ensure more reliable detection. A data bit is required to immediately follow the start gap. In the preferred embodiment, if the duration for the ensuing data bit is approximately 24 field clocks, the data bit is a zero (0). If the duration for the data bit is approximately 56 field clocks, the data bit is a one (1). In the event one or more of the data bits are not valid '0' or '1' (e.g., the duration is not within acceptable range for a zero or a one), it is assumed that no write command is actually involved and transponder 102 immediately enters into read mode. A field gap supposes to follow the first data bit followed by a second data bit. In the event there is no gap detected more than 64 field clocks after the previous gap, it is interpreted as an error and transponder 102 immediately enters into a read mode.

The first and second data bits (data packets) of the write mode data sequence constitute a write mode operation code (op-code). In other words, two data packets combine to represent a write mode operation code. There are four recognized write mode operation codes: '00', '01', '10', and '11' each representing a particular write operation. In the preferred embodiment, the first X data packets (data bits) of the write mode data sequence combine to represent a write mode operation code wherein X has a value of two (2). However, X may have any value. Op-code '00' represents a reset command. Op-code '01', wherein MAXBLK must also be '00', indicates a page write command used for testing memory cells whereby, except for block 0 and those memory blocks with an asserted lock bit, the value one (1) is written to all memory locations. Op-code '10' represents a 3-bit addressing write operation. In general, op-code '10' is followed by a lock bit indicating whether the memory block is to be overwritten once programmed, 32 data bits, and 3 address bits to select a memory block between 0-7 to write to. Accordingly, there are a total of 38 bits in the write mode sequence for a write operation involving an op-code '10'. Op-code '11' represents a 5-bit addressing write operation. Op-code '11' is generally followed by a lock bit indicating whether the memory block is to be overwritten once programmed, 32 data bits, and 5 address bits to select a memory block between 0-31 to write to. Accordingly, there are a total of 40 bits in the write mode sequence for a write operation involving an op-code '11'. If the number of bits received associated with a particular op-code is incorrect (e.g., a total of 37 bits are received for a write mode sequence involving op-code '10'), it is interpreted as an error and causes transponder 102 to switch to read mode.

FIG. 9 illustrates, as an example, the differential voltage between pads 312 and 313 in write mode in accordance to the present invention. As shown in FIG. 9, a steady voltage pattern representing the step of loading block 0 is immediately followed by an intermittent voltage pattern representing the write mode data sequence. Conversely, for comparison purposes, FIG. 10 illustrates, as an example, the differential voltage between pads 312 and 313 in read mode in accordance to the present invention. By interrupting the RF field from reader/encoder 101, dampened voltages can be created. In the preferred embodiment, such modulation is created through the use of modulator 309 which dampens the differential voltage between pads 312-313 when a RF read data signal is being sent.

Referring now back to FIG. 8, if it is determined, based on the write mode data sequence, that a write command is involved, programming data received from

reader/encoder 101 is stored in input register 306 (step 806). The programming instructions and information from the write mode sequence are utilized in programming the data into the desired memory block and in setting the lock bit. The programming voltage Vpp is measured, the lock bit from the memory block to which the data is to be programmed is examined, and the number of bits involved in a write operation is counted (steps 807-809, respectively). Vpp is continually monitored and regulated throughout the programming cycle. If Vpp does not meet the threshold voltage required to program the data into memory 310, transponder 102 immediately enters read mode (step 810). If the lock bit from the memory block to which data is to be programmed is asserted to prevent data from being written into it, transponder 102 halts the programming and immediately enters into read mode. If the number of bits related to a particular op-code is incorrect, transponder 102 also immediately enters into read mode. In other words, if all of the following occurs: 1) write command detected, 2) sufficient Vpp voltage, 3) correct number of bits detected for op-codes '10' and '11' and 4) no assertion of lock bit in memory block to which data is written, data is written into the selected block of memory 310 (step 811). At the conclusion of the programming, transponder 102 enters read mode (step 810).

Under the present invention, configuration (mode) block 0 can also be reprogrammed with new configuration settings provided that its lock bit has not been asserted. If configuration block 0 is reprogrammed, the new configuration settings are applied to subsequent read transactions.

In the preferred embodiment, read mode is the default mode. As discussed earlier, any error detected during write mode causes transponder 102 to enter into read mode. However, read mode (step 810) may also be the intended operation by reader/encoder 101 as with a continuous waveform from electrostatic reader/encoder 101 or at the conclusion of a data write/programming. If transponder 102 enters into read mode, a determination is made as to whether read mode is intended (e.g., by reader/encoder 101 or following step 811), or defaulted by errors during programming (e.g., lock bit of addressed block is asserted, Vpp is below threshold, invalid op-code, invalid '0' or '1' data bit, invalid number of bits received for a particular op-code, etc.) (step 812). If read mode is indeed intended, data is retrieved from memory 310 starting at block 1 and continues through MAXBLK (step 813). If read mode is defaulted by errors, data is retrieved from memory 310 starting at current block and continues through MAXBLK (step 817).The data retrieval cycle then

repeats continuously. Next, it is determined from mode register 308 whether modulation information bit is enabled (step 814). If modulation bit is disabled indicating no modulation is required, no data is sent to transponder electrodes 314-316 to send to reader/encoder 101 (step 815). If modulation bit is enabled indicating that modulation is required, the data is sent to modulator 309 which has been informed of the modulation scheme desired (Manchester or PSK) (step 816). Modulator 309 modulates the data and sends the modulated data to analog interface module 301 (step 816) which relays it to pads 312-313 to send to reader/encoder 101 over the transponder electrodes. While a read operation is performed, gap detector 405 continues monitoring whether a start gap has been detected in the incoming data sequence (step 803).

On the other hand, if read mode is defaulted by errors during programming, data is retrieved from memory 310 starting with the currently addressed memory block and continues through MAXBLK (step 817). Subsequently, data is retrieved from memory 310 starting with block 1 and continues through MAXBLK. The data retrieval cycle then repeats continuously. Next, it is determined from the modulation bit in mode register 308 whether modulation is enabled (step 814). If modulation bit is disabled indicating no modulation is required, no data is sent to transponder electrodes 314-316 to send to reader/encoder 101 (step 815). If modulation bit is enabled indicating that modulation is required, the data is sent to modulator 309 which has been informed of the modulation scheme desired (Manchester or PSK) (step 816). Modulator 309 modulates the data and sends the modulated data to analog interface module 301 (step 816) which relays it to pads 312-313 to send to reader/encoder 101 over the transponder electrodes. While a read operation is performed, gap detector 405 continues monitoring whether a start gap has been detected in the incoming data sequence (step 803).

An embodiment of the present invention, a contactless electrostatic programmable RFID system, apparatus, and method is thus described. Because electrodes (i.e., plates) are used (instead of coils) to transmit and receive electrostatic signals, capacitance-based RFID technology can be implemented in an integrated circuit. The electrodes and associated electrical circuits of electrostatic RFID systems can easily be implemented on flat and printable surfaces including paper, plastic, or synthetic substrates. Moreover, the manufacturing process involved is inexpensive and requires minimal components and set-up. As such, advantages of the contactless electrostatic programmable RFID system described in the present invention are its low

costs, ease of manufacturability, and packaging flexibility. These advantages make it practical to use such a contactless electrostatic programmable RFID system in high volume and low cost applications such as disposable applications.

While the present invention has been described in particular embodiments, the present invention should not be construed as limited by such embodiments, but rather construed according to the claims below.

What is claimed is:

CLAIMS

1. An electrostatic Radio Frequency Identification (RFID) reader/encoder comprising:

a processor;

an exciter coupled to the processor; and

at least one first electrode coupled to the exciter, the exciter electrostatically generating and transmitting a RF exciter signal over the at least one first electrode, the exciter further generating and transmitting a data sequence signal and a clock signal, the data sequence signal carrying a data sequence received from the processor, the data sequence indicates whether write mode is involved, the data sequence is composed of a sequence of alternating blanking gaps and pulses, the pulses representing binary values and their duration determining whether it is a zero (0) or a one (1), wherein the data sequence indicates a write operation if the data sequence begins with a blanking gap.

2. The electrostatic RFID reader/encoder of claim 1 further comprising:

a receiver coupled to the processor;

at least one second electrode coupled to the receiver, the receiver receiving an electrostatic RF read data signal from the at least one second electrode; and

a demodulator coupled to the receiver and the processor, the demodulator receiving the electrostatic RF read data signal, the demodulator demodulating the electrostatic RF read data signal prior to sending it to the processor.

3. An electrostatic RFID transponder comprising:

a plurality of electrostatic electrodes;

an analog interface module coupled to the plurality of electrostatic electrodes, the analog interface module extracting an exciter signal, a clock signal, and a data sequence signal from a RF signal received by the plurality of electrostatic electrodes, the analog interface module rectifying and regulating the exciter signal for use in activating the electrostatic RFID transponder, the analog interface module determining whether a write or a read operation is involved;

a memory;

a modulator coupled to the analog interface module, and the memory; and a controller coupled to the analog interface module and the memory, the controller writing data information from the data sequence signal into the memory in response to a write command, the controller reading data information from the memory in response to a read command and sending the data information to the modulator, the modulator modulating the data information, the modulator sending a modulated data signal to the analog interface module for sending over the plurality of electrostatic electrodes.

4. The electrostatic RFID transponder of claim 3, wherein the memory is organized into a plurality of memory blocks of L bits, wherein a memory block is used to store configuration (mode) information and other memory blocks are used to store data information and memory block locking information.

5. The electrostatic RFID transponder of claim 4, wherein the configuration (mode) information in the memory block comprises memory block locking information.

6. The electrostatic RFID transponder of claim 4, wherein the configuration (mode) information in the memory block comprises data rate information.

7. The electrostatic RFID transponder of claim 4, wherein the configuration (mode) information in the memory block comprises modulation type information.

8. The electrostatic RFID transponder of claim 4, wherein the configuration (mode) information in the memory block comprises modulation on/off information.

9. The electrostatic RFID transponder of claim 4, wherein the configuration (mode) information in the memory block comprises max block information.

10. The electrostatic RFID transponder of claim 4, wherein the configuration (mode) information in the memory block comprises and modulation threshold information.

11. A method to program an electrostatic RFID transponder in an electrostatic RFID system, the method comprising:

electrostatically transmitting a RF exciter signal to activate the electrostatic RFID transponder; and

electrostatically transmitting a RF signal carrying a data sequence received from a processor following the RF exciter signal, the data sequence indicates whether write mode is involved, the data sequence is composed of a sequence of alternating blanking gaps and pulses, the pulses representing binary values and their duration determining whether it is a zero (0) or a one (1), wherein the data sequence indicates a write operation if the data sequence begins with a blanking gap.

12. The method of claim 11, wherein the data sequence further includes instruction, data, and address information related to a write operation.

13. The method of claim 12, wherein the data sequence is transmitted a predetermined time after the RF exciter signal.

14. The method of claim 13, wherein X data packets in the data sequence combined to represent a write mode operation code.

15. The method of claim 14, wherein X has a value of two (2).

16. The method of claim 15, wherein there are four recognized write mode operation codes: '00', '01', '10', and '11'.

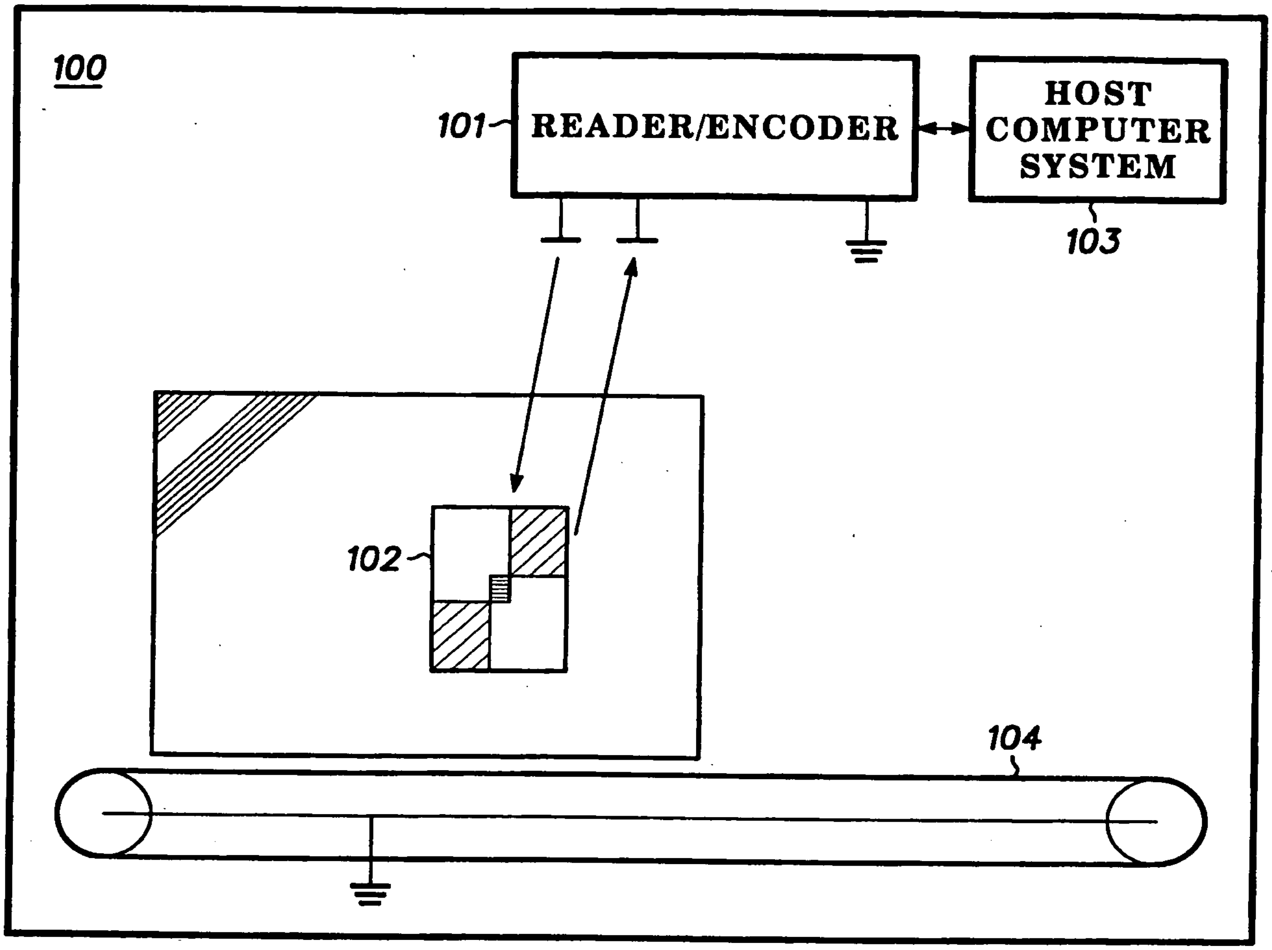

100
101
READER/ENCODER
HOST COMPUTER SYSTEM
103
102
104

FIG. 1

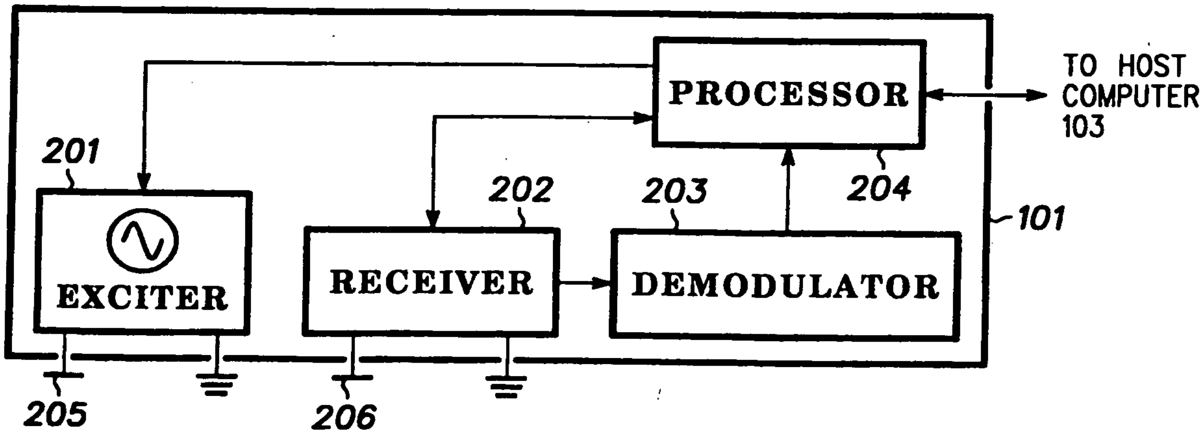
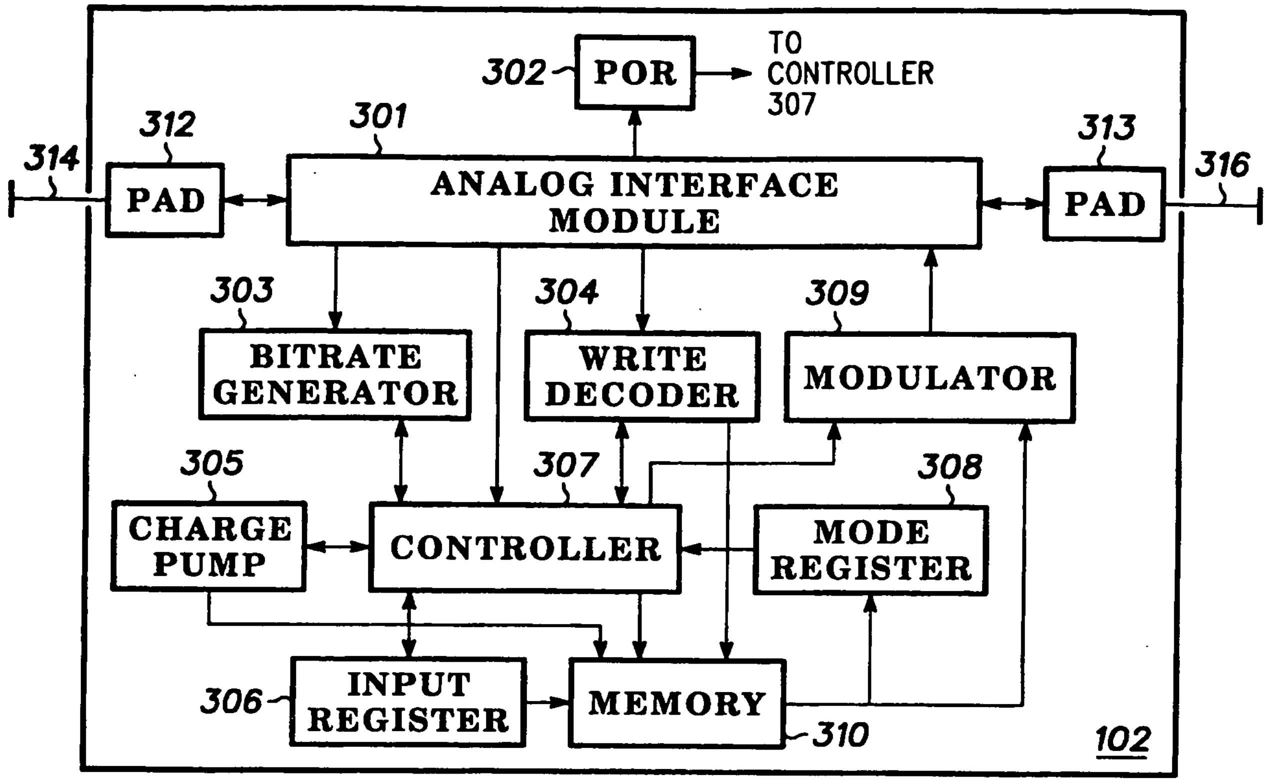
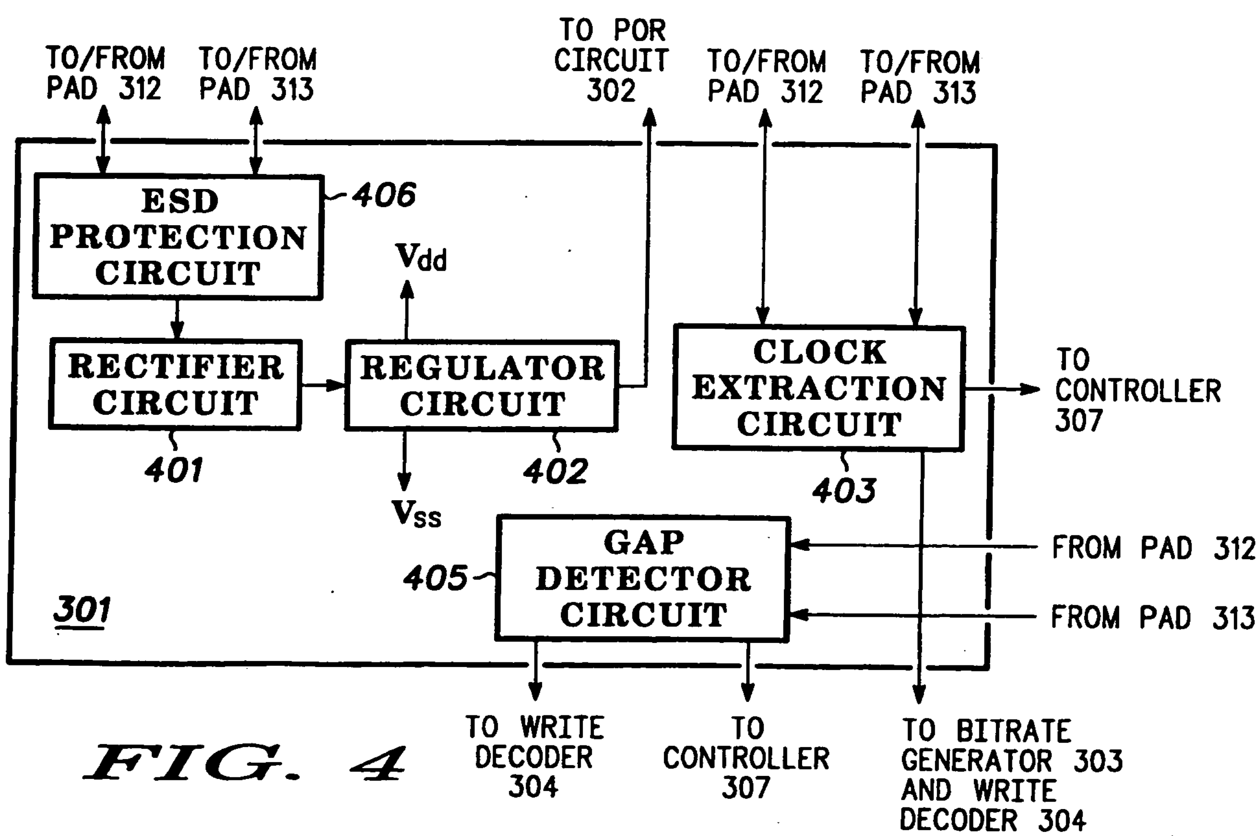

PROCESSOR
TO HOST COMPUTER 103
201
202
203
204
101
EXCITER
RECEIVER
DEMODULATOR
205
206

FIG. 2



302
POR
TO CONTROLLER 307
301
312
314
PAD
ANALOG INTERFACE MODULE
313
316
PAD
303
BITRATE GENERATOR
304
WRITE DECODER
309
MODULATOR
305
CHARGE PUMP
307
CONTROLLER
308
MODE REGISTER
306
INPUT REGISTER
MEMORY
310
102

FIG. 3



TO/FROM PAD 312
TO/FROM PAD 313
TO POR CIRCUIT 302
TO/FROM PAD 312
TO/FROM PAD 313
ESD PROTECTION CIRCUIT
406
Vdd
RECTIFIER CIRCUIT
REGULATOR CIRCUIT
CLOCK EXTRACTION CIRCUIT
TO CONTROLLER 307
401
402
Vss
403
GAP DETECTOR CIRCUIT
405
FROM PAD 312
FROM PAD 313
301
TO WRITE DECODER 304
TO CONTROLLER 307
TO BITRATE GENERATOR 303 AND WRITE DECODER 304

FIG. 4

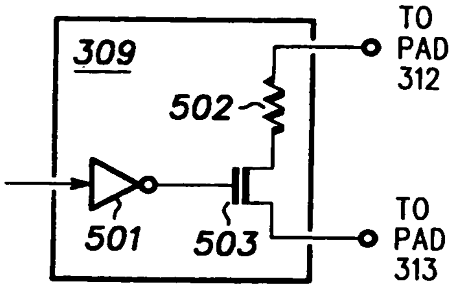


FIG. 5

0	1 ---------------	--------------- L	
L	CONFIGURATION BITS		BLOCK 0
L	SYNC. BITS	USER DATA BITS	BLOCK 1
L	SYNC. BITS	USER DATA BITS	BLOCK 2
⋮	⋮		⋮
L	SYNC. BITS	USER DATA BITS	BLOCK 29
L	SYNC. BITS	USER DATA BITS	BLOCK 30
L	SYNC. BITS	USER DATA BITS	BLOCK N

FIG. 6

0	1	2	3	4	5 -------------	------------- L
LOCK BIT	POR DELAY	DATA RATE	MOD. TYPE	MOD. ENABLE	MOD. LEVEL	MAX BLOCK ('MAXBLK')

FIG. 7

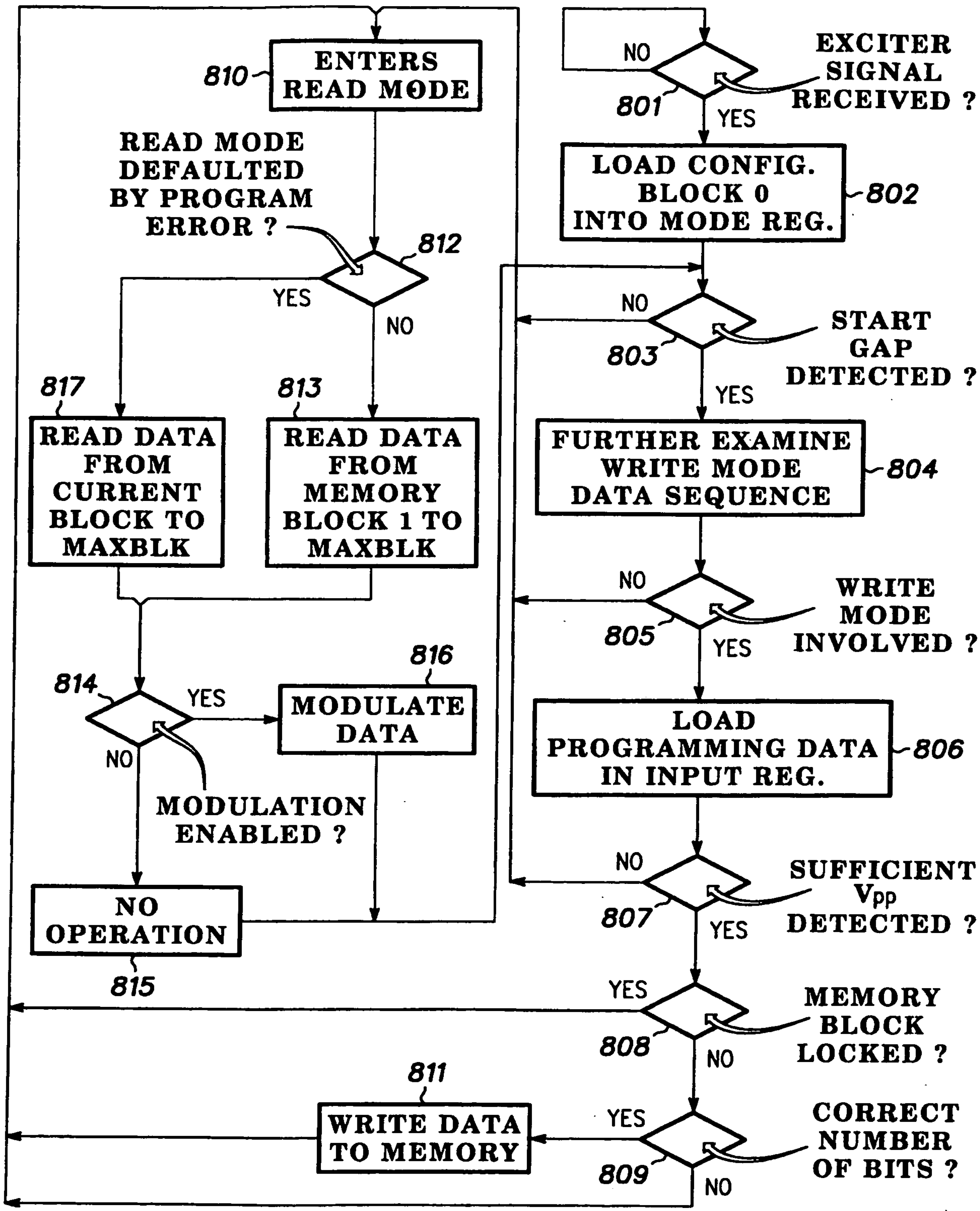

ENTERS READ MODE
810
READ MODE DEFAULTED BY PROGRAM ERROR ?
812
YES
NO
817
READ DATA FROM CURRENT BLOCK TO MAXBLK
813
READ DATA FROM MEMORY BLOCK 1 TO MAXBLK
814
YES
NO
MODULATION ENABLED ?
816
MODULATE DATA
NO OPERATION
815
NO
EXCITER SIGNAL RECEIVED ?
801
YES
LOAD CONFIG. BLOCK 0 INTO MODE REG.
802
NO
START GAP DETECTED ?
803
YES
FURTHER EXAMINE WRITE MODE DATA SEQUENCE
804
NO
WRITE MODE INVOLVED ?
805
YES
LOAD PROGRAMMING DATA IN INPUT REG.
806
NO
SUFFICIENT Vpp DETECTED ?
807
YES
YES
MEMORY BLOCK LOCKED ?
808
NO
811
WRITE DATA TO MEMORY
YES
CORRECT NUMBER OF BITS ?
809
NO

FIG. 8

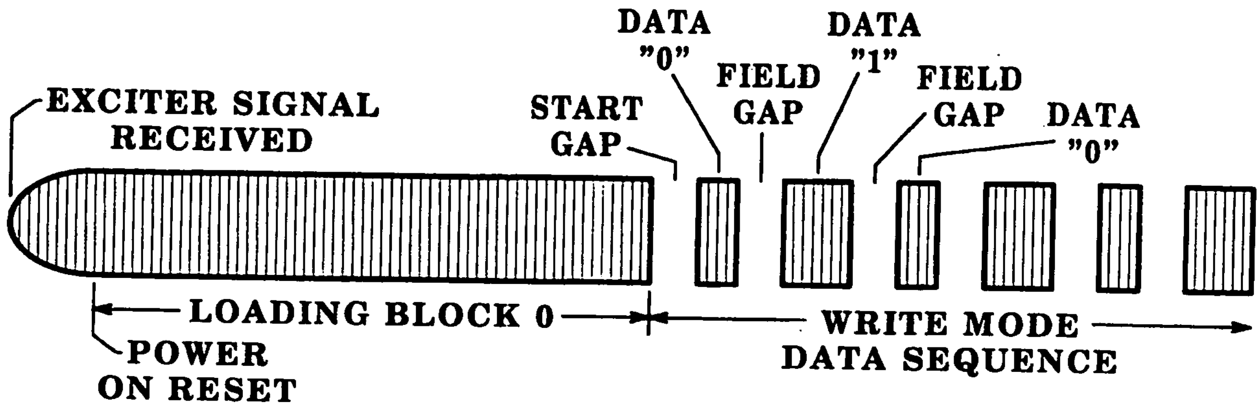

EXCITER SIGNAL RECEIVED
START GAP
DATA "0"
FIELD GAP
DATA "1"
FIELD GAP
DATA "0"
LOADING BLOCK 0
POWER ON RESET
WRITE MODE DATA SEQUENCE

FIG. 9

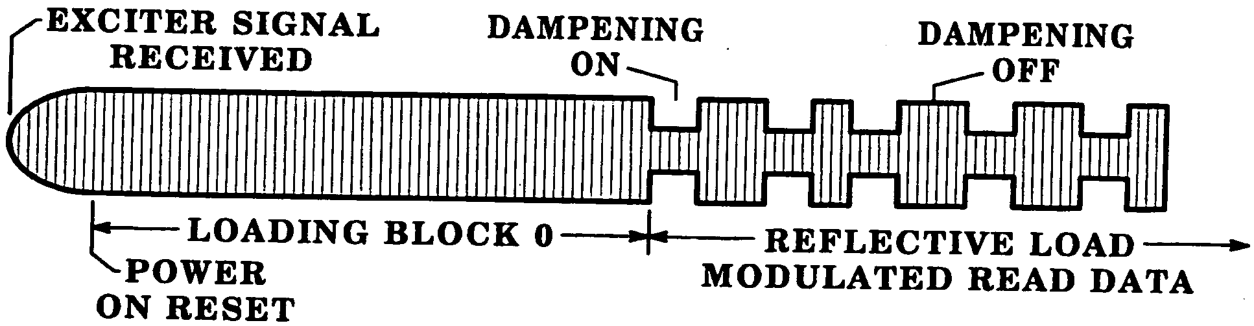

EXCITER SIGNAL RECEIVED
DAMPENING ON
DAMPENING OFF
LOADING BLOCK 0
POWER ON RESET
REFLECTIVE LOAD MODULATED READ DATA

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/20799

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.
US CL :340/825.54, 825.34, 572.1, 825.69, 825.72; 235/380; 342/44, 42
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/825.54, 825.34, 572.1, 825.69, 825.72; 235/380; 342/44, 42

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,055,659 A (HENDRICK et al) 08 October 1991, abstract and figure 1	1-16
A	US 5,521,590 A (HANAOKA et al) 28 May 1996 abstract	1-16
A,P	US 5,847,662 A (YOKOTA et al) 08 December 1998, see abstract	1-16
A,E	US 5,966,082 A (COFINO et al) 12 October 1999, abstract	1-16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 NOVEMBER 1999	07 DEC 1999

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	For Reugonia Zoyan BRIAN ZIMMERMAN
Facsimile No. (703) 305-3230	Telephone No. (703) 305-3900

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/20799

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (6):

HO4Q 7/00